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Multiplexer Using  
Cmos Ternary  
Logic

# Design Of Multiplexer Using Cmos Ternary Logic

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### Multiplexer Using

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## Design Of Multiplexer Using Cmos

4-1-multiplexer\_using\_  
CMOS\_logic | Pass-  
Transistor-Logic. 4:1  
multiplexer using  
CMOS logic The path  
selector logic Boolean  
expression can be  
given as :  $Out = AS + B\bar{S}$ . When the select  
line signal S is high A is  
passed to the output  
and when S is low B is

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CMOS Ternary  
Logic

passed to the output.  
The same logic is used  
for 4 : 1 MUX in which  
number of inputs are  
four (A, B, C, D) and  
the number of select  
lines are two (S1, S2).

**4-1-multiplexer-  
using-CMOS-logic  
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...

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CMOS design NMOS works as pull down network and PMOS works as pull up network. Fig. 6 Schematic of 2 to 1 multiplexer using NAND gates Fig.7 shows the standard cell multiplexer layout design. Standard cell multiplexer design is complex and consumes more area. Fig.7

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standard cell layout  
Design of 2 to 1  
Multiplexer  
Complementary  
Logic

**Layout Design and  
Simulation of CMOS  
Multiplexer**

Multiplexer is  
designed... (PDF) CMOS  
Design of 2:1  
Multiplexer Using  
Complementary ... 2.  
Logic design styles  
Multiplexer circuit:  
2.1.1:4:1 multiplexer  
using Conventional  
CMOS: A Multiplexer

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sends one of  $2^n$  input lines to a single output line. A Multiplexer has four sets of input  $X(0)$ ,  $X(1)$ ,  $X(2)$ ,  $X(3)$  and two select lines  $S(0)$  and  $S(1)$ . The Multiplexer output is in a single bit  $Y$  [9].

Design And Analysis of 4:1 Multiplexer Using An Efficient ... CMOS Circuit "Hybrid" a b c b

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### Multiplexer Using

### III. Ternary Multiplexer

It is a most important standard logic design. It is one of the special designs of combinational circuit which has several input and single output like 2:1, 4:1 and 8:1 multiplexer. As we can see in Fig.7 to select respective input we make the use of select line. Fig7 shows block diagram of a multiplexer with

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**Design of  
MULTIPLEXER using  
CMOS Ternary Logic**

This is basically explained by the fact that CPL gates uses less transistors, have smaller capacitances, and are faster than gates in complementary CMOS. In this paper 2:1 Multiplexer is designed...

**(PDF) CMOS Design  
of 2:1 Multiplexer**

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### Multiplexer Using

#### Using

#### Complementary ...

2. Logic design styles

Multiplexer circuit:

2.1.1:4:1 multiplexer

using Conventional

CMOS: A Multiplexer

sends one of  $2^n$  input lines to a single output line. A Multiplexer has

four sets of input  $X(0)$ ,  $X(1)$ ,  $X(2)$ ,  $X(3)$  and

two select lines  $S(0)$  and  $S(1)$ . The

Multiplexer output is in a single bit  $Y$  [9].

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**Design And Analysis  
of 4:1 Multiplexer**

**Using An Efficient ...**

CMOS Circuit "Hybrid"

a b c b a a c d c d GND

$F = ab + a'b + a'c' +$

$cd + cd$  The N and P

networks are NOT

duals, but the

switching functions ...

D Latch Design

§ Multiplexer chooses D

or old Q 9/11/18 1 0 D

CLK Q CLK CLK CLK

CLK Q D Q Q Page 30.

VLSI-1 Class Notes D

Flip-flop Design § Built

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Multiplexer Using  
from master and slave  
D latches 9/11/18 QM  
CLK CLK ...  
Logic

## **Lecture 4: Implementing Logic in CMOS**

Cmos design 1. CMOS  
Design 2. Introduction  
Integrated circuits:  
many transistors on  
one chip. Very Large  
Scale Integration  
(VLSI): very many  
Metal Oxide  
Semiconductor (MOS)  
transistor Fast, cheap,

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low-power transistors

Complementary:

mixture of n- and p-type leads to less power

How to build your own simple CMOS chip

CMOS transistors

Building logic gates from transistors

Transistor layout and

...

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6.2 Static CMOS Design

The most widely used

logic style is static

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complementary CMOS.  
The static CMOS style  
is really an extension  
of the static CMOS  
inverter to multiple  
inputs. In review, the  
primary advantage of  
the CMOS structure is  
robustness (i.e, low  
sensitivity to noise),  
good

## **DESIGNING COMBINATIONAL LOGIC GATES IN CMOS**

The main issue in

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designing of VLSI circuits is power consumption and area requirement In this paper Multiplexer circuit is proposed with the help of transmission gate logic using 6 transistors. Different design methodologies are used for designing of multiplexer layout. Multiplexer is essential circuit for different field of network and communication.



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**Power and Area  
Efficient Design of  
6T Multiplexer using**

...

2. Transmission Gate  
Logic Design 3. X-Gate  
2-to-1 MUX 4. X-Gate  
XOR 5. X-Gate 8-to-1  
MUX 6. X-Gate Logic  
Latch 7. Voltage Drop  
of n-CH X-Gates 8. n-  
CH Pass Transistors vs.  
CMOS X-Gates 9. n-CH  
Pass Transistors vs.  
CMOS X-Gates 10. Full  
Swing n-CH X-Gate

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Logic 11. Leakage  
Currents 12. Static  
CMOS Digital Latches  
13. Static CMOS Digital  
Latches 14.

**Class 11:  
Transmission Gates,  
Latches**

The CMOS TGL is used to design a new 4:1 MUX. The designed circuit is realized in 45 nm technology, with the power consumption of 1.887 nW from a 0.7 V supply voltage under

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27 °C. The leakage current is also reduced to 2.237 nA from 29.6 mA. The rise and fall time for the simulation is 100 fs.

**High performance,  
low power 200 Gb/s  
4:1 MUX with TGL in**

...

Generate the RTL schematic for the 4:1 MUX and simulate the design code using testbench. What is a multiplexer? A

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multiplexer is a data selector device that selects one input from several input lines, depending upon the enabled, select lines, and yields one single output. ... CMOS - IC Design Course

**Verilog code for 4:1 Multiplexer (MUX) - All modeling styles**

Question: Design A 1:4 De-Multiplexer ; A. Write The Logic Expression For The

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Output, Also Write The Truth Table And Realize The 1:4 De-Multiplexer Circuit Using Static CMOS Transistor. (30 Marks)

B. Draw The Stick Diagram Of 1:4 De-Multiplexer Circuit; (30Marks) C.

Appropriate Device Sizing Can Result In Equal And Symmetrical Drive Current Which Leads To A Sunstainable...

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**Solved: Design A 1:4  
De-Multiplexer; A.  
Write The Logic E ...**

SPPU BE ETC VLSI

Desin PR- Layout  
design & simulation of  
2:1 Mux using logic  
gates & transmission  
gates.

**VLSI Design PR7  
CMOS 2 :1 mux  
design using logic  
gates &TG**

The MAX4051/MAX405  
2/MAX4053 and MAX40  
51A/MAX4052A/MAX40

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### Multiplexer Using

53A are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (MAX4051/A), two 4-channel multiplexers (MAX4052/A), and three single-pole/double-throw (SPDT) switches (MAX4053/A). The A-suffix parts are fully characterized for on-resistance match, on-resistance flatness, and low leakage.

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**MAX4051 Low-  
Voltage, CMOS  
Analog Multiplexers/  
Switches ...**

1: Circuits & Layout  
CMOS VLSI Design  
Slide 3 A Brief History  
1958: First integrated  
circuit -Flip-flop using  
two transistors -Built  
by Jack Kilby at Texas  
Instruments

**Lecture 2 Circuits  
and Layout - Home |  
University of ...**

If you will write down



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the logic equations for  
a 4 to 1 multiplexor,  
then the logic will  
become obvious. For  
example, a 2-1 mux  
with select line S,  
output Y, and inputs A  
and B might be  $Y = (S$   
and A) or (not S and B)  
and the obvious  
implementation...

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ecf8427e.  
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