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CHAPTER 4 SOLUTIONS 9 effort should be about 4. This design has imbalanced delays and excessive efforts. The path effort is $F = 12 * 6 * 9 = 648$. The best number of stages is 4 or 5. One way to speed the circuit up is to add a buffer (two inverters) at the end. The gates should be resized to bear efforts of $f = 648 / 5 = 3.65$ each.

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EE 460R: Introduction to VLSI Design

The extensively revised 3rd edition of CMOS VLSI Design details modern techniques for the design of complex and high performance CMOS Systems-on-Chip. The authors draw upon extensive industry and classroom experience to explain modern practices of chip design. The introductory chapter covers transistor operation, CMOS gate design, fabrication, and layout at a level accessible to anyone with an elementary knowledge of digital electronics.

Weste & Harris, CMOS VLSI Design: A Circuits and Systems ...

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David Money Harris Associate Professor of Engineering at Harvey Mudd College in Claremont, CA, holds a Ph.D. from Stanford University and S.B. and M.Eng. degrees from MIT. His research interests include CMOS VLSI design, microprocessors, and computer arithmetic. He holds a dozen patents, is the author of three other books in the field of digital design and three hiking guidebooks, and has ...

Weste & Harris, CMOS VLSI Design: A Circuits and Systems ...

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Introduction to CMOS Image Sensors - Florida State University

CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition) Neil Weste ... for an issue titled "New Circuit and Architecture-Level Solutions for Multidiscipline Systems," August 2012, and IET Circuits, Devices & Systems (CDS) for an issue titled "Design Methodologies for Nanoelectronic Digital and Analog Circuits," September 2013 ...

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